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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Dmitriy Rumynin et al.

Title: A PARALLEL COUNTER AND A LOGIC CIRCUIT FOR PERFORMING MULTIPLICATION

Docket No.: 1365.051US1
Filed: July 27, 2001
Examiner: Unknown

Serial No.: 09/917,257
Due Date: N/A
Group Art Unit: 2121

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

We are transmitting herewith the following attached items (as indicated with an "X"):

X A return postcard.
X A Communication Concerning Related Applications (2 pgs.).
X A Supplemental Information Disclosure Statement (2 pgs.), Form 1449 (1 pg.), and copies of 9 cited documents.

If not provided for in a separate paper filed herewith, Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Customer Number 21186

By: [signature]
Atty: Timothy B Clise
Reg. No. 40,957

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 19TH day of July, 2004.

JAMES KANYUSIK
Name

[signature]
Signature

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
(GENERAL)

S/N 09/917,257 PATENT

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Applicant:	Dmitriy Rumynin et al.	Examiner: Unknown
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COMMUNICATION CONCERNING RELATED APPLICATIONS

MS Amendment
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P.O. Box 1450
Alexandria, VA 22313-1450

Applicants would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

Serial/Patent No.	Filing Date	Attorney Docket	Title
09/637532	August 11, 2000	1365.033US1	A PARALLEL COUNTER AND MULTIPLICATION LOGIC CIRCUIT
09/769954	January 25, 2001	1365.039US1	A PARALLEL COUNTER AND A MULTIPLICATION LOGIC CIRCUIT
10/472658	September 22, 2003	1365.072US1	A MULTIPLICATION LOGIC CIRCUIT
10/714408	November 14, 2003	1365.063US1	LOGIC CIRCUIT AND METHOD FOR CARRY AND SUM GENERATION AND METHOD OF DESIGNING SUCH A LOGIC CIRCUIT
10/776938	February 11, 2004	1365.065US1	LOGIC CIRCUITS FOR PERFORMING THRESHOLD FUNCTIONS

10/817752	April 2, 2004	1365.085US1	A PARALLEL COUNTER AND A LOGIC CIRCUIT FOR PERFORMING MULTIPLICATION

Respectfully submitted,

DMITRIY RUMYNIN ET AL.

By Applicants' Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 349-9587

Date 19 July '04 By

Timothy B. Clise
Reg. No. 40,957

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JAMES KANYUSIK
Name

Signature

S/N 09/917,257 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Dmitriy Rumynin et al.	Examiner:	Unknown
Serial No.:	09/917,257	Group Art Unit:	2121
Filed:	July 27, 2001	Docket:	1365.051US1
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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Supplemental Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Supplemental Information Disclosure Statement considered.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

DMITRIY RUMYNIN ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 349-9587

Date 19 July '04 By ______________________
Timothy B Clise
Reg. No. 40,957

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JAMES KANYUSIK
Name

____
Signature

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	09/917,257
Filing Date	July 27, 2001
First Named Inventor	Rumynin, Dmitriy
Group Art Unit	2121
Examiner Name	Unknown

Attorney Docket No: 1365.051US1

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US-6,175.852	01/16/2001	Dhong, S. H., et al.	708	712	07/13/1998
	US-6,269,386	07/31/2001	Siers, S. E., et al.	708	710	10/14/1998

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T[2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		BEDRIJ, O. J., "Carry-Select Adder", IRE Trans., EC-11, (June 1962),340-346	
		KNOWLES, S. , "A Family of Adders", Proc. 14th IEEE Symp. on Computer Arithmetic, (1999),30-34	
		KOGGE, P. M., et al., "A Parallel Algorithm for the Efficient Solution of a General Class of Recurrence Equations", IEEE Trans. Computers, Vol. C-22, No. 8, (Aug. 1973),786-793	
		LADNER, RICHARD E., et al., "Parallel Prefix Computation", Journal of ACM, Vol. 27, No. 4, (Oct. 1980),831-838	
		LING, HUEY , "High-Speed Binary Adder", IBM Journal of Research and Development, Vol. 25, No. 3, (1981),156-166	
		SKLANSKY, J., "Conditional-Sum Addition Logic", IRE Trans., EC-9, (June 1960),226-231	
		WEINBERGER, A., et al., "A Logic for High-Speed Addition", Nat. Bur. Stand. Circ., 591, (1958),3-12	

EXAMINER

DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached